

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/56	Serial No. 10/009,649
	Applicant(s) Martin Vorbach et al.	
	Filing Date May 29, 2002	Group Art Unit 2192

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,627,992	May 6, 1997	Baror			
	6,049,866	April 11, 2000	Earl			
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	7,028,107	April 11, 2006	Vorbach et al.			
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	2002/0156962	October 24, 2002	Chopra et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	2001-167066	June 22, 2001	Japan			Abstract	
	11-184718	July 9, 1999	Japan			Abstract	
	5-265705	October 15, 1993	Japan			Abstract	

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EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.	
	Altera, "APEX 20K Programmable Logic Device Family," Altera Corporation Data Sheet, March 2004, ver. 5.1, pp. 1-117.	
	IMEC, "ADRES multimedia processor & 3MF multimedia platform," Transferable IP, IMEC Technology Description, (Applicants believe the date to be October 2005), 2 pages.	
	Kanter, David, "NVIDIA's GT200: Inside a Parallel Processor," http://www.realworldtech.com/page.cfm?ArticleID=RW090989195242&p=1 , September 8, 2008, 27 pages.	
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," (v2.2) September 10, 2002, Xilinx Production Product Specification, pp. 1-52.	
	XILINX, "Virtex-II and Virtex-II Pro X FPGA Platform FPGAs: Complete Data Sheet," (v4.6) March 5, 2007, pp. 1-302.	
	XILINX, "Virtex-II Platform FPGAs: Complete Data Sheet," (v3.5) November 5, 2007, pp. 1-226.	
EXAMINER	/Thuy Dao/	DATE CONSIDERED 03/30/2010
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		